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(54) A semiconductor device using a lead frame and its manufacturing method.

(57) A plurality of electrode pads (14) are formed on a main surface of a semiconductor chip (11). The electrode pads (14) on the semiconductor chip (11) are electrically connected to the top end of an inner lead (19) through a metal plating layer (20).

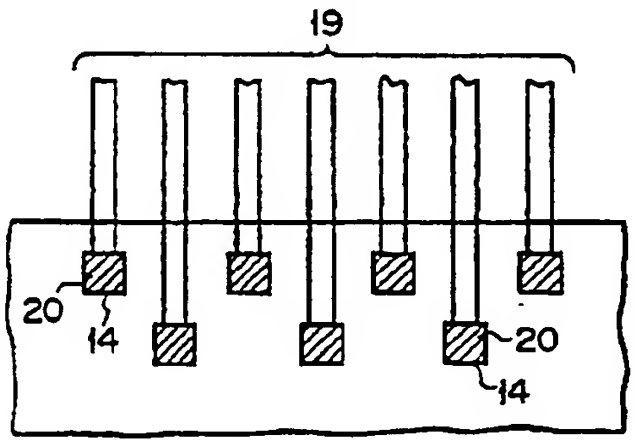

FIG. 7

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an electrolytic plating solution and forming a metal plating layer where the lead frame is electrically connected to the electrode on the semiconductor chip.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a cross sectional view showing the structure of a part of a device of a first embodiment of the present invention;

Fig. 2 is a cross sectional view showing a general structure of the device of the first embodiment of the present invention;

Fig. 3 is a cross sectional view showing a specific structure of an electrode pad of the device of the first embodiment of the present invention;

Fig. 4 is a plane view showing a state of the connection between a plurality of electrode pads of the device of the first embodiment and a plurality of inner leads;

Figs. 5 and 6 are plane views of a TAP tape, which is used in the device of the first embodiment of the present invention, respectively;

Figs. 7 and 8 are plane views of modifications of the device of the first embodiment of the present invention, respectively;

Fig. 9 is a cross sectional view showing a device of a second embodiment of the present invention;

Fig. 10 is a cross sectional view showing a device of a third embodiment of the present invention; and

Fig. 11 is a cross sectional view showing a device of a fourth embodiment of the present invention.

The embodiments of the present invention will be explained with reference to the drawings.

Fig. 1 shows the structure of a part of a semiconductor device of a first embodiment of the present invention wherein the present invention is used in the connection between a plurality of electrode pads on a semiconductor chip and a plurality of inner leads, and Fig. 2 is the general structure thereof.

In the drawings, reference numeral 11 is a semiconductor chip wherein an active element such as a transistor and a passive element such as a resistor and a capacity. Around the main surface of the semiconductor chip 11, there are formed a plurality of electrode pads 14, which is formed of a first metal layer 12 whose lower layer is formed of aluminum (Aℓ) and a second metal layer 13 whose upper layer includes at least one nickel layer. These electrode pads 14 are arranged in line with a predetermined distance. The portions of the semiconductor chip 11 other than the electrode pad formation position are covered with an insulating surface protection film 15 such as a silicon oxidation film. The semiconductor chip 11 is adhered to a predetermined portion of a TAB tape 17 by an epoxy adhesive 16.

As shown in Fig. 1, the TAB tape 17 is made of epoxy or polyimide resin. Metal foil such as copper (Cu) foil having a thickness of about 35 μm is laminated on an organic film material 18 having a thickness of about 75 μm. Thereafter, there is formed a wiring pattern comprising a plurality of inner leads 19 to be connected to the plurality of electrode pads 14 by a selection etching technique and outer leads electrically connected to these inner leads (not shown). The wiring pattern forming surface is adhered to the semiconductor chip 11 by the adhesive 16.

When the semiconductor chip 11 is adhered to the TAB tape 17, the positioning is performed in a state that each electrode pad 14 is positioned close to the portion where each end surface of the end portions of the plurality of inner leads 19 is exposed. Then, each electrode pad 14 on the semiconductor chip 11 and each end portion of the inner lead 19 are electrically connected through a metal plating layer 20 formed of nickel (Ni).

Fig. 3 shows the specific structure of each electrode pad 14. In this embodiment, the second metal layer 13 formed on the first metal layer 12 made of aluminum (Aℓ) comprises at least two metal layers. More specifically, the lower layer contacting the first metal layer made of aluminum is formed of a titan (Ti) layer 31 having a thickness of 1000 Å, and the upper layer is formed of the nickel (Ni) layer 32 having a thickness of 3000 Å. The nickel layer 32, which is the upper layer of the second metal layer 13 is formed to allow the metal plating layer 20 made of nickel to be formed on the electrode pad 14. Also, the titan layer 31, which is the lower layer of the second metal layer 13, has a function as barrier metal.

Fig. 4 shows a state of the connection between the plurality of electrode pads 14 and the plurality of inner leads 19 formed on the TAB tape 17. In the drawing, a region in which slant lines are added shows the metal plating layer 20.

In the above embodiment, each electrode pad 14 on the semiconductor chip 11 and each inner lead 19 are connected by the metal plating layer 20. Due to this, bonding capillary and TAB tool, which are used to the wire bonding and TAB connection are not required. Thereby, the distance between electrode pads 14 can be reduced to 100 μm or less, for example, about 50 μm.

Moreover, if each electrode pad 14 and each inner lead 19 are electrically connected, no physical pressure is applied to the semiconductor chip 11, so that reliance due to pressure damage is not lowered. Then, since a large number of portions

can be connected at the same time under the same condition, reliance of connection can be improved. Moreover, since there is no need of heating when the connection is performed, it is possible to prevent reliance from being lowered by thermal stress, which is caused by a mismatch of tho coefficient of thermal expansion of each semiconductor layer in the semiconductor chip.

A method of forming the above metal plating layer where the electrode pads and the inner leads are electrically connected will be explained.

In TAB tape, as shown in Fig. 5, metal foil such copper foil is laminated on the organic film material 18 in advance. Thereafter, in every semiconductor device, there are formed a plurality of lead electrodes 41 comprising the inner leads and the outer leads connected to the inner leads by the selection etching technique. At the same time when the selection etching is performed, common electrodes 42, which are electrically connected to the lead electrodes 41, are formed around each semiconductor device in a state that all common electrodes 42 are connected. Additionally, in Fig. 5, reference numeral 43 is an opening formed in the organic film material 18.

Fig. 6 shows an enlarged one semiconductor device in the TAB tape of Fig. 5 in the drawing, the semiconductor chip is adhered to TAB tape in a state that the semiconductor chip is positioned in the area shown by a one dotted chine line. In this case, the semiconductor chip is adhered to TAB tape so that the pad of each electrode on the semiconductor chip is positioned close to the portion where each end of the end portion of the plurality of leads is exposed.

Thereafter, TAB tape is immersed in nickel plating bath together with a plating electrode. The nickel plating bath is generally called a watt bath, and nickel sulfate, nickel chloride, and adhesive are used. After TAB tape and the plating electrode are immersed in the watt bath, a predetermined direct voltage is applied between the common electrode 42 and the plating electrode in order that the common electrode 42 serves as a positive side and the plating electrode serves as a negative side, and electrolytic plating is performed for a predetermined period of time. For example, a direct voltage to be applied was set to 2V, a current to be supplied between the positive and negative sides was set to 60mA, and plating time was set to 10 minutes. As a result, a nickel plating layer having a thickness of 10 µm was obtained as metal plating layer 20. The metal plating layer grows from each end surface of the top end portion of the inner lead immediately after plating starts. Then, if the growth advances and the plating layer contacts the electrode pad on the semiconductor chip, the metal layer also grows in the electrode pad, and both the common electrode 42 and the plating electrode are finally electrically connected by the plating layer. After the end of plating, the plating layer is washed with pure water, and contaminant, which was adhered to the surface when plating, is removed. Additionally, in the surface of each lead electrode 41, which comprises the inner and outer leads, the most of the surface other than the top end portion of the inner lead is coated with an epoxy insulating film, which is called green coat. Thereby, it is possible to form the plating layer in only the necessary portion. Due to this, plating time can be shortened.

Various modifications of the first embodiment will be explained.

The above embodiment explained that the electrode pads were arranged in line with a predetermined distance. In the modified device of Fig. 7, the electrode pads 14 are arranged on the semiconductor chip in a zig-zag manner. The same reference numerals as Fig. 4 are added in the portions corresponding to the portions of Fig. 4, and the explanation thereof is omitted.

Fig. 8 shows a modification of the device using a semiconductor which is the so-called free access pad layout system wherein the electrode pads are arranged on the entire surface of the semiconductor chip at random.

As mentioned above, the present invention can be used in any type of chip regardless of the arrangement of the electrode pads on the chip.

Next, other embodiments of the present invention will be explained.

Fig. 9 shows the structure of the semiconductor device relating to a second embodiment of the present invention wherein the present invention is used in the connection between the outer leads of the lead frame and the wiring pattern on the print circuit board. In the drawing, reference numeral 11 is a semiconductor chip, and reference numeral 17 is a TAB tape. In this embodiment, the top end portion of the inner lead of the TAB tap and electrode pad (not shown) on the semiconductor chip 11 are electrically connected by a metal plating layer 20 similar to the first embodiment. According to the second embodiment, a wiring pattern 52, which is formed on a print circuit board 51, and the outer lead of the TAB tape are also electrically connected by the metal plating layer 20.

Fig. 10 shows the structure of the semiconductor device relating to a third embodiment of the present invention wherein the present invention is used in the connection between the outer leads of the lead frame and the wiring pattern on the print circuit board. According to the third embodiment, the lead frame is formed by punching a metal thin film, which is formed of alloy such as 4-2 alloy and copper by a press process. An inner lead 53 of the

lead frame and an electrode pad 14 on a semiconductor chip are electrically connected by use of both a conductive adhesive 54 and a metal plating layer 55. In the case of the first embodiment using the TAB tape, the metal plating layer can be formed in a manner that the semiconductor chip is adhered to the TAB tape by the adhesive in advance. In the case of using the lead frame formed by punching the metal thin film, the adhesive 54 is formed on each electrode pad 14 in advance by a screen printing method and the electrode pad 14 and the lead frame 53 are adhered by the adhesive 54. Thereafter, the plating layer 55 is formed by the same method as mentioned above, and both the electrode pad and the lead frame can be electrically connected.

As mentioned above, the present invention can be used in not only the connection between the inner lead of the lead frame and the electrode pad on the semiconductor chip but also the connection between the outer lead and the wiring pattern on the print circuit board, and the same effect can be obtained. Moreover, the present invention can be used in the electrical connection between a liquid crystal display and TAB tape.

The present invention is not limited to the above-mentioned embodiments. It is needless to say that the present invention can be variously modified. For example, in the above embodiments explained the case wherein the metal plating layer was the nickel plating layer. According to the present invention, Au plating layer and copper plating layer can be used in addition to the above case.

The above first embodiment explained the case wherein the most of the surface other than the top end portion of the inner lead was coated with the insulating film in advance. However, in the portion other than the top end portion of the inner lead, the thickness of which the plating layer can grow on the above portion is about only 1/10 times that of the top end portion when the electrolytic plating is performed, the adherence of the insulating film can be omitted.

Moreover, the method of the above embodiment explained the case that the plating layer was formed by the electrolytic plating method. However, the plating layer can be formed by an electroiessly plating method.

Fig. 11 is a cross sectional view showing a device of a fourth embodiment of the present invention. The above embodiments explained the case in which two wirings are connected to each other by the plating metal. However, this plating metal can be used as a sealing for the semiconductor device. The device of the fourth embodiment shows that the plating layer is used as a sealing for a cap of a PGA (Pin Grid Array) typed semiconductor device. In Fig. 11, a package 61 is formed by layering tow ceramic plates 62 and 63. On one ceramic plate 62, a concave portion 64 is formed, and a semiconductor chip 65 is contained in the concave portion 64. Also, a plurality of wirings 66, 66, ... are formed on the surface of one ceramic plate 62. Moreover, there are formed a plurality of pads (not shown) on the surface of the semiconductor chip 65. Then, the plurality of pads on the semiconductor chip 65 and the plurality of wirings 66, 66 ... are connected by metal wires 67, 67 ..., respectively.

On the other ceramic plate 63, there is formed an opening 68 having an area larger than the concave portion 64 at the position corresponding to the concave portion 64 of one ceramic plate 62. The opening 68 forms the concave portion 64 and the containing section of the semiconductor chip 68. Then, on the surface of the ceramic plate 63 around the opening 68, there is formed, for example, an Fe - Ni metal layer 69. Moreover, the opening 68 of the ceramic plate 63 is covered with a cap 70. The metal layer 69 and the cap 70 are adhered to each other by a metal plating layer 71 formed of nickel. The metal plating layer 71 is also formed between the cap 70 and the metal layer 69 and on the entire exposed surface.

As mentioned above, the metal plating layer can be used as a sealing for the cap.

Claims

1. A semiconductor device characterized by comprising:
   a lead frame (19; 53) formed of a conductive material;
   a semiconductor chip (11) having a plurality of electrodes (14) on its surface; and
   a connect section (20) where said lead frame is electrically connected to said plurality of electrodes on the semiconductor chip by a metal plating.

2. The semiconductor device according to claim 1, characterized in that said lead frame (19) is a TAB type in which a wiring pattern is formed on an insulating film (18).

3. The semiconductor device according to claim 1, characterized in that said lead frame (53) is formed by punching a metal film.

4. The semiconductor device according to claim 1, characterized in that said plurality of electrodes (14) formed on the surface of said semiconductor chip comprise an aluminum layer (12), a titan layer (31) formed on said aluminum layer (12), one layer (32) of a metal

layer formed on said titan layer, a nickel layer, or a copper layer.

5. The semiconductor device according to claim 1, characterized in that said plurality of electrodes are arranged on said semiconductor chip in a zig-zag manner.

6. The semiconductor device according to claim 1, characterized in that said plurality of electrodes are arranged on said semiconductor chip at random.

7. A semiconductor device characterized by comprising:

an insulating film (18);

a wiring pattern (19) formed on said insulating film;

a semiconductor chip (11) having a plurality of electrodes (14) on its surface; and

a connect section (20) where the end surface of said wiring pattern is electrically connected to said plurality of electrodes on said semiconductor chip by a metal plating.

8. The semiconductor device according to claim 7, characterized in that said plurality of electrodes (14) formed on the surface of said semiconductor chip comprise an aluminum layer (12), a titan layer (31) formed on said aluminum layer (12), one layer (32) of a metal layer formed on said titan layer, a nickel layer, or a copper layer.

9. The semiconductor device according to claim 8, characterized in that said plurality of electrodes are arranged on said semiconductor chip in a zig-zag manner.

10. The semiconductor device according to claim 8, characterized in that said plurality of electrodes are arranged on said semiconductor chip at random.

11. A semiconductor device characterized by comprising:

a semiconductor chip (11);

a plurality of leads (17) electrically connected to said semiconductor chip;

a wiring board (51) having a wiring pattern (52) on its surface; and

a plurality of connect sections (20) where said plurality of leads are electrically connected to said wiring pattern on said wiring board by a metal plating.

12. A semiconductor device characterized by comprising:

a lead frame (53) formed of a conductive material;

a semiconductor chip (11) having an electrode (14) on its surface;

a first connect section (54) where said lead frame is electrically connected to an electrode on said semiconductor chip by a conductive adhesive; and

a second connect section (55) where said lead frame is electrically connected to said electrode on said semiconductor chip by a metal plating to cover the surroundings of said first connect section.

13. A method of manufacturing a semiconductor device comprising the steps of:

moving a lead frame (19) formed of a conductive material and an electrode (14) formed on a surface of a semiconductor chip (11) to be close to each other, and adhering said semiconductor chip to said lead frame; and

immersing said lead frame and said semiconductor chip in an electrolytic plating solution, and forming a metal plating layer where said lead frame is electrically connected to said electrode on said semiconductor chip.

14. The method according to claim 13, characterized in that said lead frame (19) is formed of a plurality of lead electrodes (41), said plurality of lead electrodes (41) are electrically connected by a common electrode (42), and an electric potential is supplied to said common electrode (42) when said metal plating layer is formed.

15. A semiconductor device characterized by comprising:

a package (61) formed of an insulating material and having a containing portion (64, 68) of a semiconductor chip;

a conductive layer (69) formed around said containing portion of said case;

a cap (70) formed on said containing portion of said package; and

a metal plating layer (71) connecting said cap (70) to said conductive layer (69).

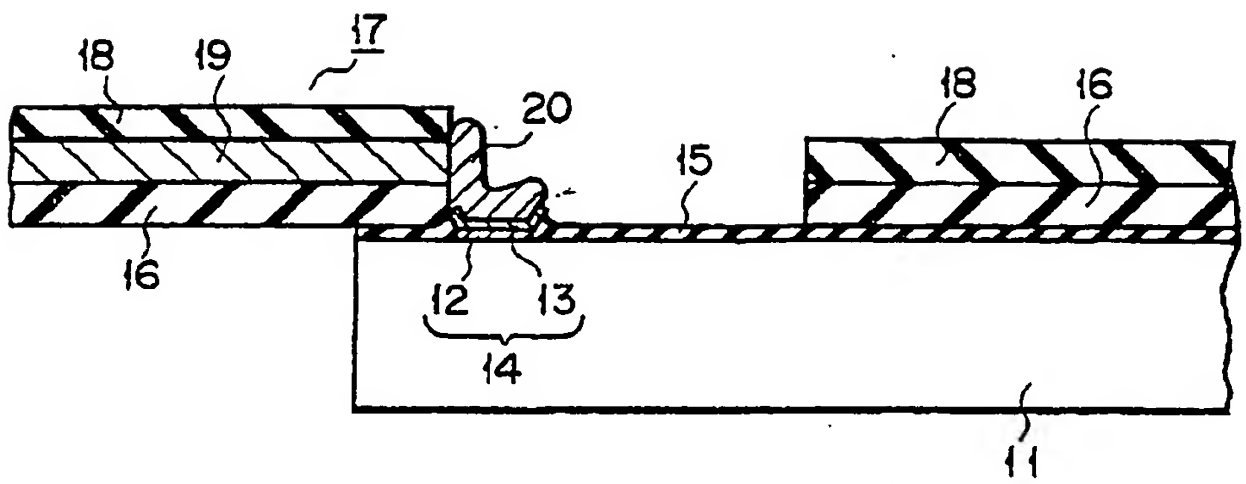

FIG. 1

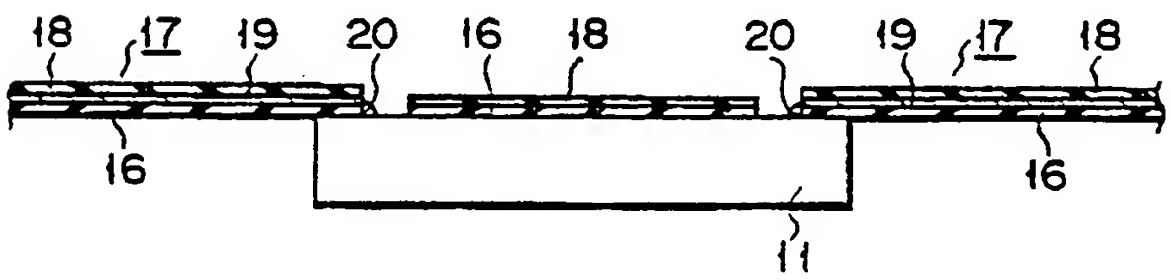

FIG. 2

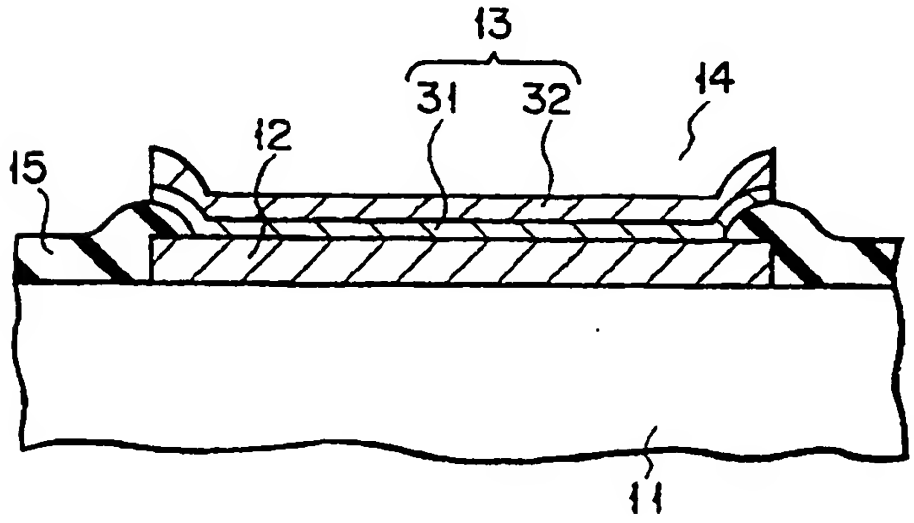

FIG. 3

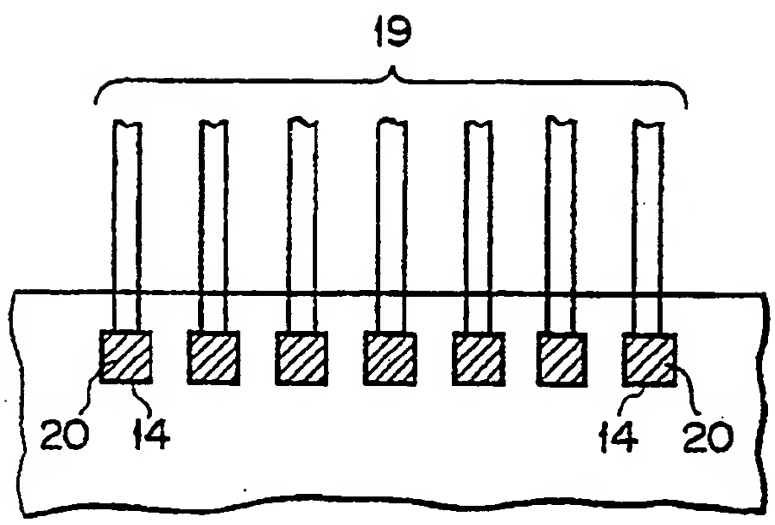

FIG. 4

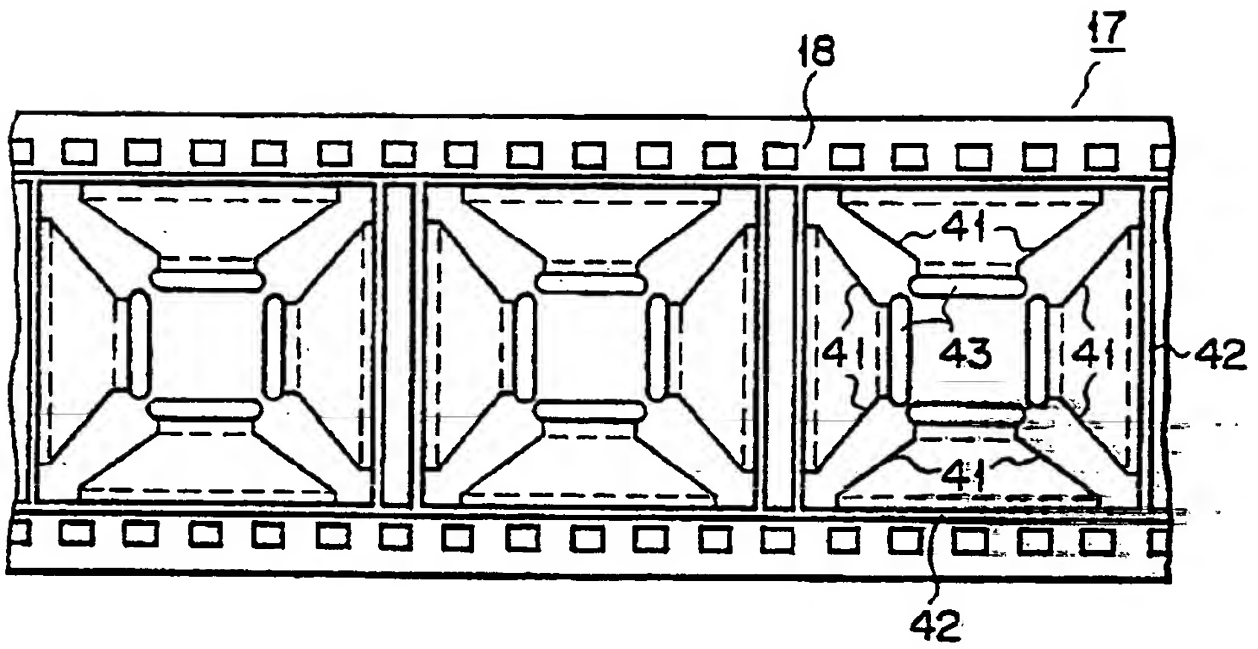

FIG. 5

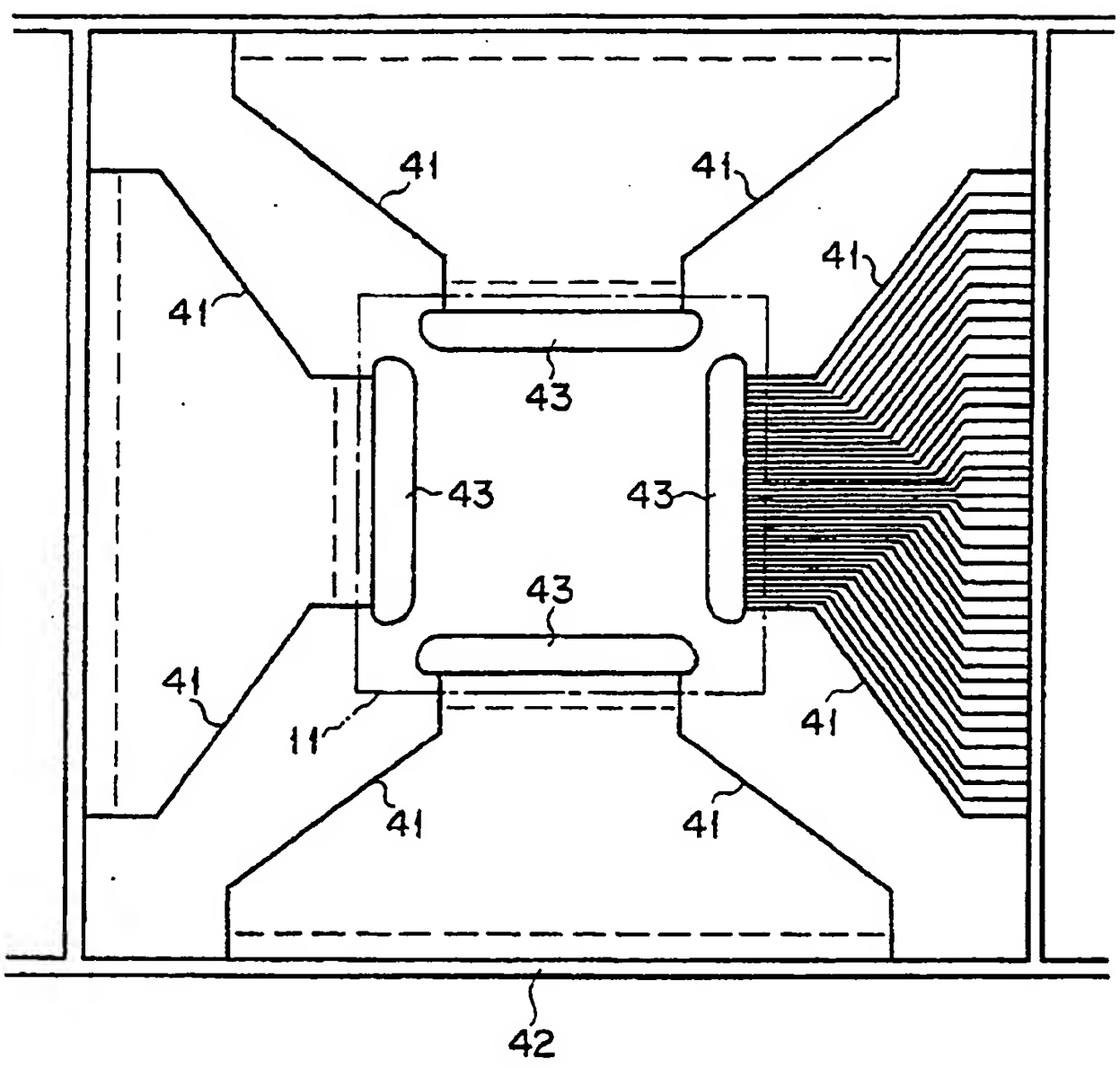

FIG. 6

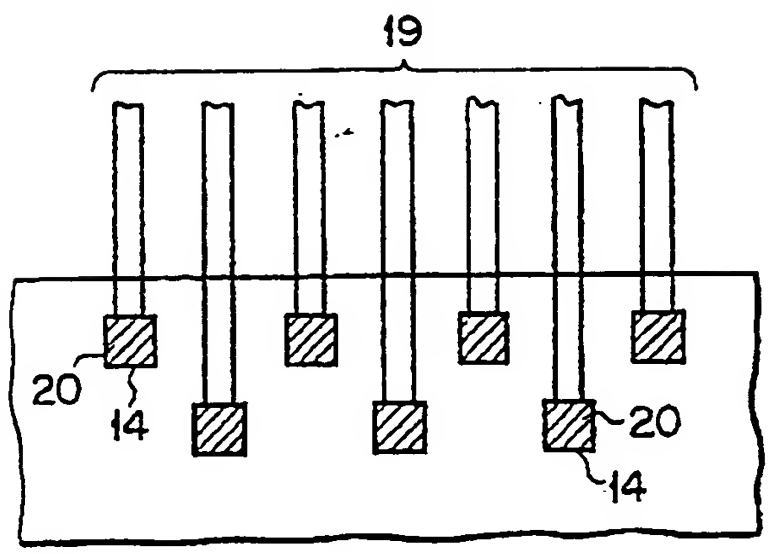

FIG. 7

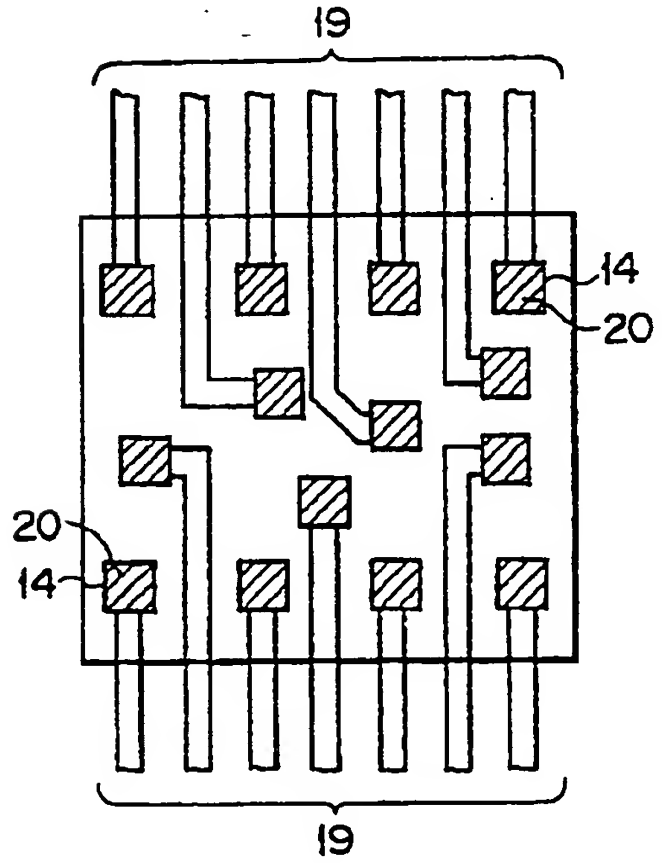

FIG. 8

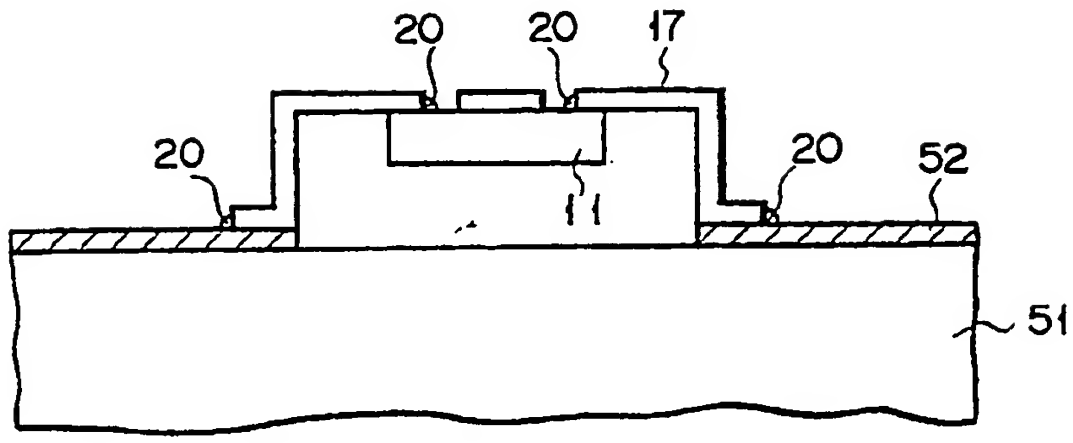

FIG. 9

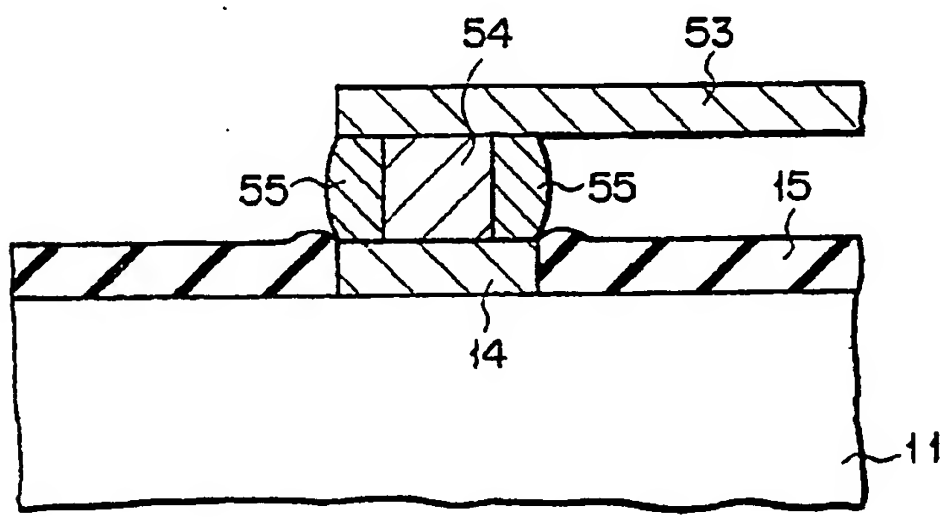

FIG. 10

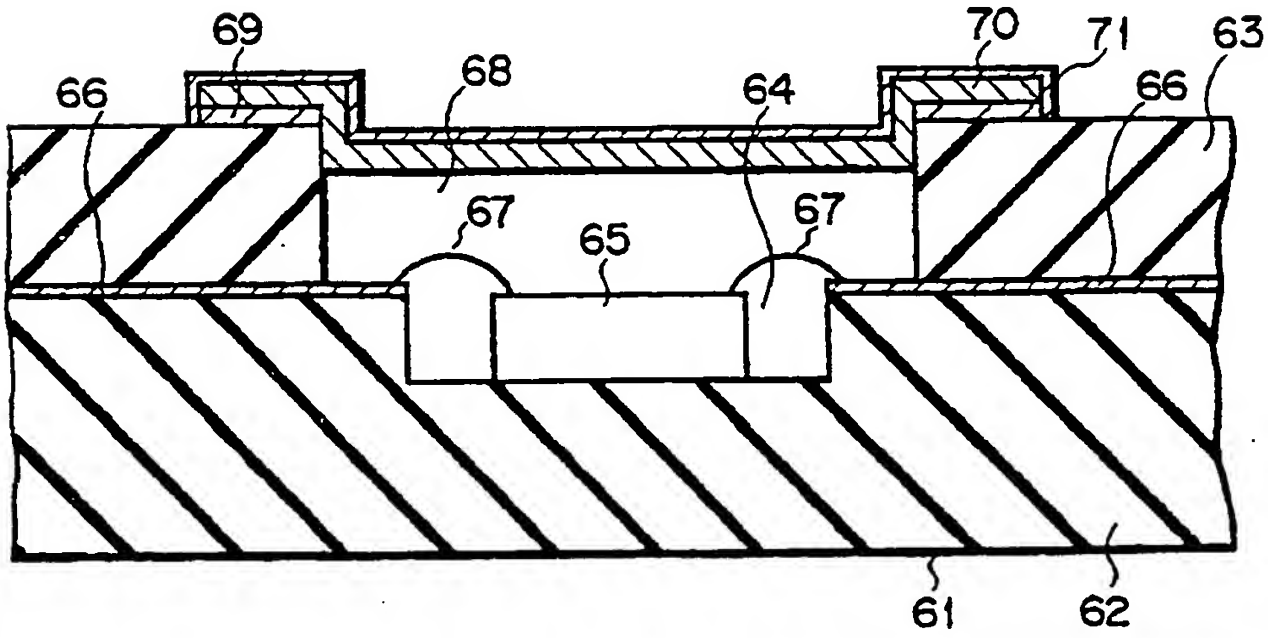

FIG. 11